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| Terms | Documents |
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| ((virtual or logical) near5 port) same concentrator | 31 |

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| <i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i> | | |
| <u>L3</u> ((virtual or logical) near5 port) same concentrator | 31 | <u>L3</u> |
| <u>L2</u> ((virtual or logical) near5 port) same concentrator same bus | 1 | <u>L2</u> |
| <u>L1</u> ((virtual or logical) near5 port) same physical same concentrator same bus | 1 | <u>L1</u> |

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L4 ((virtual or logical) near5 port) same concentrator

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 ((virtual or logical) near5 port) same concentrator

L2 ((virtual or logical) near5 port) same concentrator same bus

L1 ((virtual or logical) near5 port) same physical same concentrator same bus

Hit Count Set Name

result set

1 L4

31 L3

1 L2

1 L1

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Search Results -

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|---------------------|-----------|
| L1 and concentrator | 0 |

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| DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR | | | |
| <u>L4</u> | L1 and concentrator | 0 | <u>L4</u> |
| DB=PGPB,USPT,USOC; PLUR=YES; OP=OR | | | |
| <u>L3</u> | L1 same concentrator | 1 | <u>L3</u> |
| <u>L2</u> | L1 and concentrator | 36 | <u>L2</u> |
| <u>L1</u> | ((virtual or logical) near10 port) same bus | 1197 | <u>L1</u> |

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|--------------|---------------------|--|
| Term: | L1 and concentrator |   |
|--------------|---------------------|--|

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|-----------------|---------------------------------|-------------------------------------|--------------------------------|-----------------------------|--------------------------------|
| Display: | <input type="text" value="10"/> | Documents in Display Format: | <input type="text" value="-"/> | Starting with Number | <input type="text" value="1"/> |
|-----------------|---------------------------------|-------------------------------------|--------------------------------|-----------------------------|--------------------------------|

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|-----------|---|------|-----------|
| <u>L3</u> | L1 same concentrator | 1 | <u>L3</u> |
| <u>L2</u> | L1 and concentrator | 36 | <u>L2</u> |
| <u>L1</u> | ((virtual or logical) near10 port) same bus | 1197 | <u>L1</u> |

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» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information



1. A multiprocessor architecture for high-rate communication processing

Johnson, E.E.;

Military Communications Conference, 1991. MILCOM '91, Conference Record, 'Military Communications in a Changing World', IEEE

4-7 Nov. 1991 Page(s):1001 - 1006 vol.3

Digital Object Identifier 10.1109/MILCOM.1991.258421

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2. Evaluation of Futurebus+ for a GMMP multiprocessor

Johnson, E.E.; Moore, R.S.; Polson, J.T.;

Computing and Information, 1992. Proceedings. ICCI '92., Fourth International Conference on 28-30 May 1992 Page(s):441 - 444

Digital Object Identifier 10.1109/ICCI.1992.227617

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A multiprocessor architecture for high-rate communication processing

Johnson, E.E.
New Mexico State Univ., Las Cruces, NM, USA;

This paper appears in: Military Communications Conference, 1991. MILCOM '91, Conference Record, 'Military Communications in a Changing World', IEEE

Publication Date: 4-7 Nov. 1991

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INSPEC Accession Number: 4264065

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Posted online: 2002-08-06 18:05:46.0

Abstract

The author presents a general-purpose multiprocessor architecture which accommodates an I/O bandwidth of many Gb/s through the use of VRAM in the main memory. The virtual port memory architecture is a global-memory-message-passing multiprocessor which is well suited to I/O-intensive real-time processing. This bus-based architecture permits incremental adjustments in I/O bandwidth, memory size, and processing power by simply adding or removing I/O controllers, memory modules, and processors. This architecture is described, followed by an analysis of its performance in handling various communication processing tasks, including the 4x300 Mb/s data stream at the NASA Tracking and Data Relay Satellite System (TDRSS) ground terminal

Index Terms
Inspec

Controlled Indexing

computer networks data communication systems multiprocessor systems parallel architectures satellite relay systems telecommunications computing

Non-controlled Indexing

NASATracking and Data Relay Satellite System VRAM bus-based architecture data communication global memory-message-passing multiprocessor high-rate communication processing multiprocessor architecture performance virtual port memory architecture

Author Keywords

Not Available

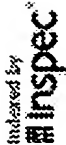
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| IEE CNF | IEE Conference Proceeding |
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